## CLAIMS

Di	1	1. A transistor comprising:
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05	Z	a substrate;
	3	a defined channel region;
	4	a floating gate generally disposed over said channel region separated therefrom by a
	5	first insulating layer;
/	6	a control gate generally placed on one side of said floating gate separated therefrom by a
$\int$	7	second insulation layer;
13 . A	8	an erase gate generally placed on a second side of said floating gate separated therefrom
	9	by said second insulation layer;
	10-	a drain region generally disposed on a first side of said floating gate; and
	11 .	a source region generally disposed on a second side of said floating gate.
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البال	1	2. A transistor as recited in claim 1 wherein said erase gate overlaps said floating gate and
<b>7</b> )	2	said control gate.
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	1	3. A method for fabricating a transistor, comprising the steps of:
	2	a) providing a substrate;
	3	b) defining a channel region;
	4	c) growing field oxide in defined areas;
	5	d) providing a first insulating layer;

depositing a first poly-silicon layer;

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- f) defining from said first poly-silicon layer a floating gate generally positioned over said channel region;
- 9 g) doping a source region;
- 10 h) providing a second insulating layer;
- i) depositing a second poly-silicon layer;
- j) defining a control gate and an erase gate; and
- 13 k) doping a drain region.
- 1 4. A method as recited in claim 3 wherein said control gate is generally positioned on a
- 2 first side of said floating gate and overlapping said floating gate.
- 1 5. A method as recited in claim 3 wherein said erase gate is generally positioned on a
- 2 second side of said floating gate and overlapping said floating gate.
- 1 6. A method as recited in claim 5 wherein said erase gate is generally positioned on said
- 2 second side of said floating gate and verlapping said floating gate and said control gate.
- 1 7. A method as recited in claim 5 wherein said erase gate is generally positioned on said
- 2 second side of said floating gate and overlapping said floating gate and about flush with said
- 3 control gate.
- 1 8. A memory array comprising a plurality of memory cells each having a floating gate, an
- 2 erase gate, a control gate, a cource region, and a drain region comprising:

- 3 a plurality of rows and columns of interconnected memory cells wherein the control
- 4 gates of memory cells in the same row are connected by a common word-line, the erase gates of
- 5 the memory cells in the same rows are connected by a common erase line, and the source
- 6 regions of the memory cells in the same rows are connected by a common source line, and the
- drain regions of memory cells in the same columns are commonly connected via a common 7
- drain line; and 8
- 9 control circuit connecting to said word-lines, erase lines, source lines and drain lines for
- operating one or more memory cells of said memory array. 10
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- A memory array as recited in claim 8 wherein each of said memory cells comprising: a 1
- 2. substrate, a defined channel region, a floating gate generally disposed over said channel region
- separated therefrom by a first insulating layer, a control gate generally placed on one side of 3
- said floating gate separated therefrom by a second insulation layer, an erase gate generally 4
- placed on a second side of said floating gate separated therefrom by said second insulation
- 6 layer, a drain region generally disposed on a first side of said floating gate, and a source region
- 7 generally disposed on a second side of said floating gate
- 1 10. A memory array as recited in claim 9 wherein said erase gate overlaps said floating gate
- and said control gate.
- A method for fabricating a memory array comprising a plurality of rows and columns of 1
- interconnected memory cells wherein/the control gates of memory cells in the same rows are 2
- 3 connected by a common word-line and the erase gates of the memory cells in the same columns

- 4 are connected by a common drase line, and the source regions of memory cells in the same
- 5 rows are connected by a common source line, and drain regions of memory cells in the same
- 6 columns are connected by a common drain lines, comprising the steps of :
- 7 a) providing a substrate;
- 8 b) defining a channel region;
- 9 c) growing field oxide in defined areas;
- d) providing a first insulating layer;
- e) depositing a first poly-silicon layer;
- 12 f) defining from said first poly-silicon layer a floating gate generally positioned
- 13 over said channel region;
- g) doping a source region;
- 15 h) providing a second insulating layer;
- i) depositing a second poly-silicon layer;
- j) defining a control gate and an erase gate; and
- 18 k) doping a drain region.
  - 1 12. A method as recited in claim 11 wherein said control gate is generally positioned on a
  - 2 first side of said floating gate and overlapping said floating gate.
  - 1 13. A method as recited in claim 11 wherein said erase gate is generally positioned on a
  - 2 second side of said floating gate and overlapping said floating gate.

- 14. A method as recited in claim 13 wherein said erase gate is generally positioned on said 1
- second side of said floating gate and overlapping said floating gate and said control gate. 2
- A method as recited in claim 13 wherein said erase gate is generally positioned on said 15. 1
- 2 second side of said floating gate and overlapping said floating gate and about flush with said
- 3 control gate.

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